REMARKS

35 U.S.C. § 102 Rejections

The Examiner has rejected claims 1-22 under 35 U.S.C. § 102(b) as being anticipated by Baker.

Claims 1 and 12 include generating primary and secondary queue heads to represent a single endpoint between high and full/low-speed devices. Specifically, claims 1 and 12 include the limitations "generating a primary interrupt queue head and a secondary interrupt queue head, the primary and secondary interrupt queue heads to represent an endpoint" and "and one of the host and the remote device is one is a high-speed device and the other is at least one of a full-speed and a low-speed device."

Baker does not disclose generating primary and secondary interrupt queue heads to represent a single endpoint between high and full/low-speed devices. Baker discloses a personal computer system that includes a digital signal processor subsystem that is connectable to a plurality of application specific hardware devices and is operable under a real-time operating system to concurrently handle a plurality of different signal processing functions on a real-time basis (Abstract). As illustrated in Fig. 1, computer 10 comprises a microprocessor 12 connected to a local bus 14 which, in turn, is connected to a bus interface controller 16, an optional math co-processor 18, and a small computer system interface adapter 20 (Col. 4, lines 9-14). Referring to Fig. 8, during operation of the system, a real-time operating system 300 is responsive to PC requests 440 and to interrupts 442 to perform multitasking in

the following general manner. The request or interrupt identifies the task to be performed and RTOS 300 accesses by step 444 the RTOS data area 322 to look up the address of the specific Task Control Block for the task (Col. 12, lines 33-39). Queue 358 includes both real-time and non-real-time tasks, the latter being executed when there are no real-time tasks remaining in the queue. Tasks are dequeued and executed from the top of the queue and as each one is dequeued, the remaining real-time tasks are moved towards the top to await their turn (Col. 12, lines 47-53). Baker thus discloses generating and initializing multiple queue heads that represents multiple tasks. Specifically, Baker does not disclose generating primary and secondary interrupt queue heads to represent a single endpoint between high and full/low-speed devices.

Therefore, claims 1 and 12 are not anticipated by Baker because claims 1 and 12 include a limitation that is not disclosed in Baker.

Claims 2, 4-8, 10-13, 15-19, 21, and 22 are dependent on either claim 1 or claim 12 and should be allowable for the same reasons stated above.

Claims 3, 9, 14, and 20 have been cancelled.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 1, 2, 4-8, 10-13, 15-19, 21, and 22 under 35 U.S.C. § 102(b) as being anticipated by Baker.

The Examiner has rejected claims 1-30 under 35 U.S.C. § 102(e) as being anticipated by Wooten.

Claims 1, 12, 23, and 28 include generating primary and secondary interrupt queue heads to represent a single endpoint between high and full/low-speed devices. Specifically, claims 1 and 12 include the limitations generating "a primary interrupt queue head and a secondary interrupt queue head, the primary and secondary interrupt queue heads to represent the endpoint" and "and one of the host and the remote device is one is a high-speed device and the other is at least one of a full-speed and a low-speed device." Claims 23 and 28 include the limitations "a primary interrupt queue head and a secondary interrupt queue head, the primary and secondary interrupt queue heads to represent the endpoint," "a high-speed host," and a "full-/low-speed remote device."

Wooten does not disclose generating primary and secondary interrupt queue heads to represent a single endpoint between high and full/low-speed devices. Wooten discloses a computer system that includes a serial bus host controller and a host controller driver that provides data structures, having linking mechanisms for processing lists of descriptors and alternate buffer configurations, for the host controller to operate on (Abstract). Each serial bus transaction begins when the host controller 330, on a scheduled basis, sends a serial bus packet describing the type of transfer, the serial bus device address, and the endpoint number (Col. 6, lines 38-41). This packet is the token packet. The serial bus endpoint that is addressed selects itself by decoding the appropriate addressed fields (Col. 6, lines 41-43). In a given transaction, data is transferred whether from the host to a device or from a device to a host. The interruption of data transfer is specified in the token packet. The source

of the transfer then sends a data packet or indicates that has no data to transfer. The destination responds with a handshake packet indicating whether the transfer was successful. (Col. 6, lines 45-49). Wooten thus discloses sending a serial bus packet for each serial bus transaction. Specifically, Wooten does not disclose generating primary and secondary interrupt queue heads to represent a single endpoint between high and full/low-speed devices.

Therefore, claims 1, 12, 23, and 28 are not anticipated by Wooten because claims 1, 12, 23, and 28 include a limitation that is not disclosed in Wooten.

Claim 2, 4-8, 10-13, 15-19, 21-26, 29, and 30 are dependent on either claim 1, claim 12, claim 23, or claim 28 and should be allowable for the same reasons as stated above.

Claims 3, 9, 14, 20, and 27 have been cancelled.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 1, 2, 4-8, 10-13, 15-19, 21-26, and 28-30 under 35 U.S.C. § 102(e) as being anticipated by Wooten.

The Examiner has rejected claims 1-30 under 35 U.S.C. § 102(e) as being clearly anticipated by Leete.

Claims 1, 12, 23, and 28 include generating primary and secondary interrupt queue heads to represent a single endpoint between high and full/low-speed devices. Specifically, claims 1 and 12 include the limitations generating "a primary interrupt queue head and a secondary interrupt queue head, the primary and

secondary interrupt queue heads to represent the endpoint" and "and one of the host and the remote device is one is a high-speed device and the other is at least one of a full-speed and a low-speed device." Claims 23 and 28 include the limitations "a primary interrupt queue head and a secondary interrupt queue head, the primary and secondary interrupt queue heads to represent the endpoint," "a high-speed host," and a "full-/low-speed remote device."

Leete does not disclose generating primary and secondary interrupt queue heads to represent a single endpoint between high and full/low-speed devices. Leete discloses a device including a host controller capable of attaching a quantity of queue heads to a frame list before any transaction descriptors (Abstract). As illustrated in Fig. 9, block 910 determines whether a queue head max packet size is less than or equal to a predetermined size and that the period is greater or equal to a predetermined scheduled window (Para. 0038). If block 910 determines that a queue head max packet size is not equal or less than a predetermined size and/or that the period is not greater or equal to a predetermined schedule window, then process 900 continues with block 950. Block 950 places the queue head in the interrupt tree. Block 940 then determines whether initialization is complete or not, and if block 940 determines that all queue heads are not processed, the process returns to block 910. (Paras. 0039 and 0040). Leete thus discloses a method for determining whether a queue head has less than or equal to a predetermined packet size and whether a period is one of greater than and equal to a predetermined window. Specifically, Leete does not disclose generating primary and secondary

interrupt queue heads to represent a single endpoint between high and full/low-speed devices.

Therefore, claims 1, 12, 23, and 28 are not anticipated by Leete because claims 1, 12, 23, and 28 include a limitation that is not disclosed in Leete.

Claims 2, 4-8, 10-13, 15-19, 21-26, 29, and 30 are dependent on either claim 1, claim 12, claim 23, or claim 28 and should be allowable for the same reasons stated above.

Claims 3, 9, 14, 20, and 27 have been cancelled.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 1, 2, 4-8, 10-13, 15-19, 21-26, and 28-30 under 35 U.S.C. § 102(e) as being clearly anticipated by Leete.

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Mark A. Kupanoff at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), Applicant hereby requests and authorizes the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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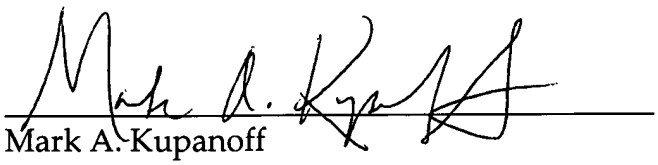

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